HYPERBITS™ Connector Design and Qualification For High Reliability Compact PCI Serial Space Applications

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ABSTRACT

With the adoption of Compact PCI Serial Architecture for Spaceflight applications, new challenges arise for hardware qualification, especially for the connectors found within the data handling system's core hardware.

Current commercial high speed connector offerings present limitations in power transfer capabilities and rely on their electrical interfaces as means for mechanical locking to PCBs, a condition which is generally regarded as a risk to long-term reliability in harsh environment applications.
In addition, it is still ambiguous as to whether hard compliant stamped press-fit contact interface technology is fully suitable for harsh environment applications as the industry has not thoroughly investigated the possible long-term impact to PCB integrity after the brutal shock and vibration conditions present during launching, and sustained cycling under rapid changes of temperature, a condition characteristic of low-orbit space environment.

INTRODUCTION

In August of 2017 the PCI Industrial Computers Manufacturers Group (PICMG) has released the CPCI Serial Space Specification CPCI-S.1 R1.0 following requests from Airbus Defense and Space, Thales Alenia Space, and other users to adopt the industry proven Compact PCI Serial Standard for avionics and communication systems in future generations of satellite constellations with the objective to save design time and cost during the development of projects and their life cycles. The flexibility offered by the CPCI Serial Standard, with the added cost benefit of modular hardware configuration flexibility, is more appealing than the VPX standard for embedded systems in space applications.

During 2020 a consortium named ADHA was formed between ADS, TAS and Ruag. ADHA stands for Advanced Data Handling Architecture and its main objective is to fully adapt the CPCI Serial Space architecture to space-bound applications.

However, the adoption of the open industrial standard to space applications does not come without some hidden challenges and the first obvious challenge is to establish if the existing commercial-grade high data-rate connectors are suitable for harsh environment applications and to determine if they conform to the performance requirements of the applicable ESCC 3401 or equivalent specifications.

Furthermore, based on limited evidence collected from past compatibility investigations [1], it appears important to consider developing a new generation of high data-rate connectors, a generation of connectors which are designed specifically to overcome the electromechanical risks inherent to commercial versions and to improve the performance characteristics making the product future-proof and align it with the gradually increasing demand in performance.

BACKGROUND

March 2021: Airbus Defense and Space released a specification defining the requirements for space-flight compatible CPCI Serial high data-rate connectors. This document is referenced as DOC-EEE-000218505.

September 2021: MINDREACH i2i SL, an IP assets generation and management firm based in Andorra, files patent application for Single-Piece High Data Rate Backplane Connector named HYPERBITS™ . The most distinguishing innovation is that HYPERBITS is a single body connector which installs on a card (PCB) and blind-mates directly with the backplane therefore eliminating the need to install a second connector on the backplane.

November 2021: MINDREACH i2i SL files patent application for S-FECT™ (Slide-Fit Electrical Contact Termination) Technology and adapts the S-FECT™ Technology to the HYPERBITS™ connector.

March 2022: MINDREACH i2i SL and ALTER TECHNOLOGY enter into collaboration agreement for the validation and the qualification of the HYPERBITS™ connector to ESCC 3401 and CPCI-S.1 R1.0.

April 2022: ESA releases an RFP for Procurement and Reliability Assessment of High Data Rate Press-Fit CPCI SS connectors in which commercial grade connectors and HYPERBITS™ are to be evaluated for conformance to ESCC 3401.

August 2022: ESA Tender Action is released under ARTES for the development of space qualified high-density electrical interconnections for CPCI-S.1 R1.0.

August 2022: MINDREACH i2i SL awards license for S-FECT™ Technology and HYPERBITS™ to PERFORMANCE INTERCONNECT SAS and opens licensing agreement availability to any connector manufacturer interested to manufacture the HYPERBITS™ connector.

December 2022: Alter Technology of Seville, Spain shall commence the evaluation activities of CPCI Serial commercial connectors and HYPERBITS™ connectors.

Slide-Fit Electrical Contact Termination (S-FECT™) Technology

Slide-Fit is an interface method achieved between cylindrical pins and sockets based on a simple operation principle employing offsetting elements on the longitudinal axis of male contacts before or after they are inserted into compatible sockets or PCB metallized holes. See figure 1 demonstrating post-insertion offset and figure 2 showing pre-insertion offset configurations.

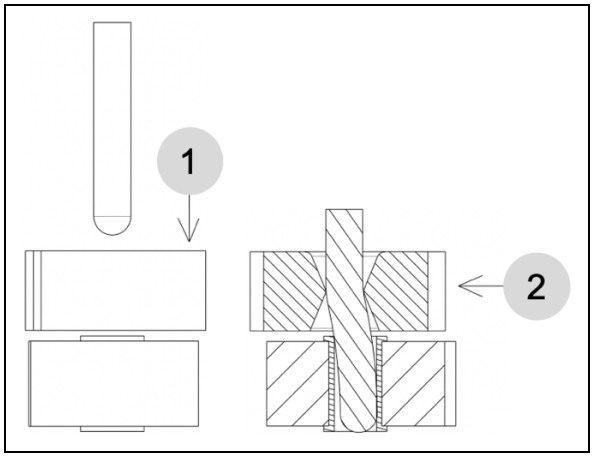

Fig. 1

Step 1: contact is inserted with zero resistance into the PCB through the aligned offsetting plate

Step 2: offsetting plate is pushed sideways to achieve normal force between contact and plated through hole

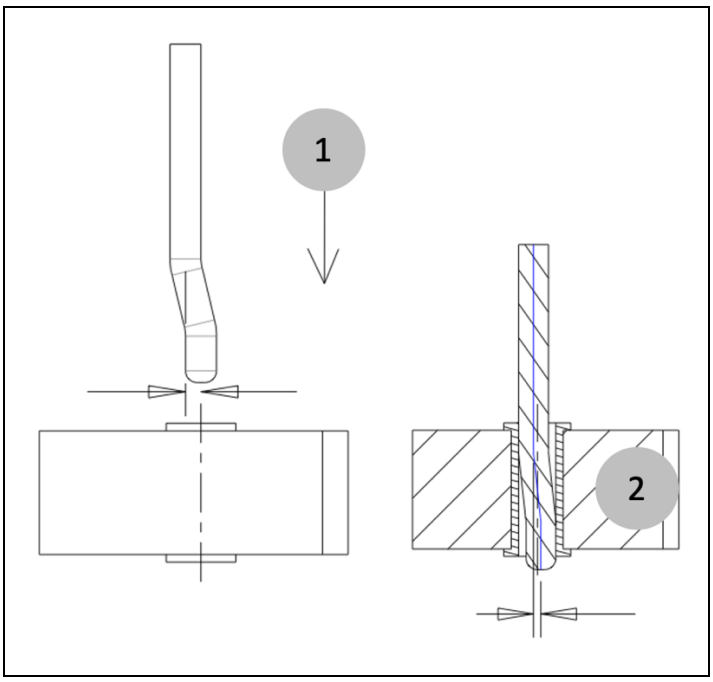

Fig. 2

Step 1: Pre-offset contact is pressed into PCB without special insertion tools

Step 2: Contact in axial elastic deformation making contact with PTH

Slide-Fit technology is designed to operate in close correlation between the pin's outer diameter and the socket's inner diameter and furthermore, the pin materials are selected based on the ability to maintain their elastic properties throughout the operating temperature rating of the final component.

Since the active interface property resides with the male contact, S-FECT™ Technology enable male contacts to connect directly with drilled sockets, directly with PCB metallized holes, with holes into busbars, etc.

When compared with traditional male-female contact interfaces where the active pressure element resides within the female contact, it becomes obvious that S-FECT™ Technology opens new opportunities to expand the range of applications towards increased miniaturization while significantly reducing the manufacturing and assembly costs of the components and their installation because of the simplicity of the S-FECT™ principle of operation.

The difference between Slide-Fit and Press-Fit Technologies

The fundamental difference between the two technologies consists in the way the interface forces are applied between the contact termination and the cylindrical cavity where it is inserted, as shown in Figure 3.

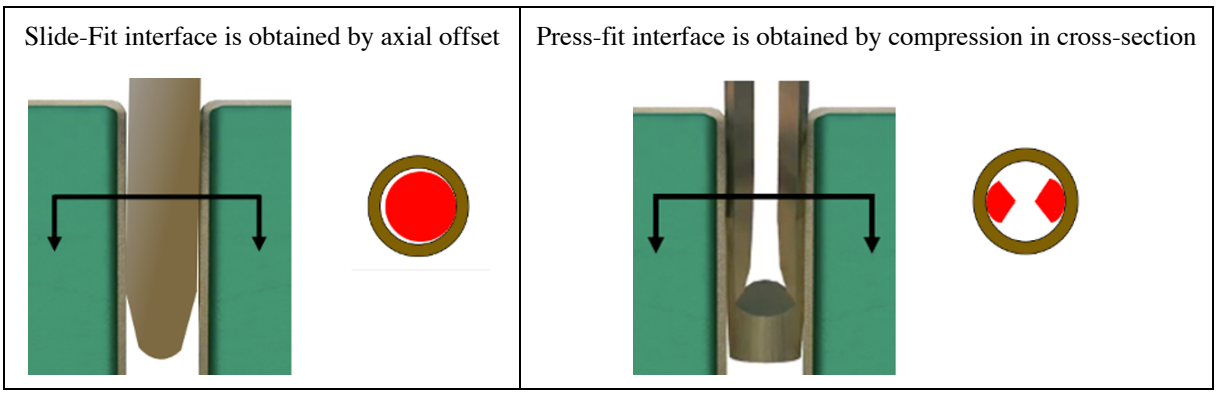

Fig. 3 – The differences between Slide-Fit and Press-Fit Technologies

There are several benefits to Slide-Fit as opposed to Press-Fit:

1. ZERO insertion force of component is possible with post-insertion offset
2. ZERO wiping or minimal wiping of the plated surface on the inner walls of the socket and on the outer walls of the contact
3. ZERO jet effect distortion on the metallized wall on PCB (refer to IEC-9797)
4. Negligeable deformation on plated-through hole as the amount of pressure is controlled by the offset distance
5. Post-insertion offset does not require inspection for metallic particles after insertion
6. High insertion-removal cycling without effect on plated surfaces
7. Elimination of insertion and removal tools
8. Reduced manufacturing cost
9. Miniaturization is easier to accomplish since the contact diameter remains constant through the active zone
10. Improved thermal behavior since the material mass through the zone of interface is not reduced

The HYPERBITS™ Connector

HYPERBITS™ is an innovative single-piece PCB to PCB direct blind-mating connector designed for harsh environment CPCI Serial Space applications. The design embodies several innovations in interconnect technology including the use of S-FECT™ Technology on both sides of the connection system. The HYPERBITS™ connector eliminates the conventional two-piece connection system known as male to female or plug to socket and blind-mates directly into the via holes on the backplane with a sophisticated self-aligning post-insertion offsetting system.
The connector installation on the card (daughterboard) is achieved without any special tooling and the zero-insertion-force design permits for high count of insertion-removal cycles which makes possible the reutilization of the connectors on subsequent equipment generations in retrofittable systems. As a state-of-the-art electromechanical device, the HYPERBITS™ connector fully separates the mechanical function from the electrical function on both sides of the interconnection. The S-FECT™ Technology allows the HYPERBITS™ connector to achieve the best performance to price ratio in the spectrum of high-reliability for harsh environment applications.

The connector and the underlying S-FECT Technology are shown in detail in Figures 4 through 13.

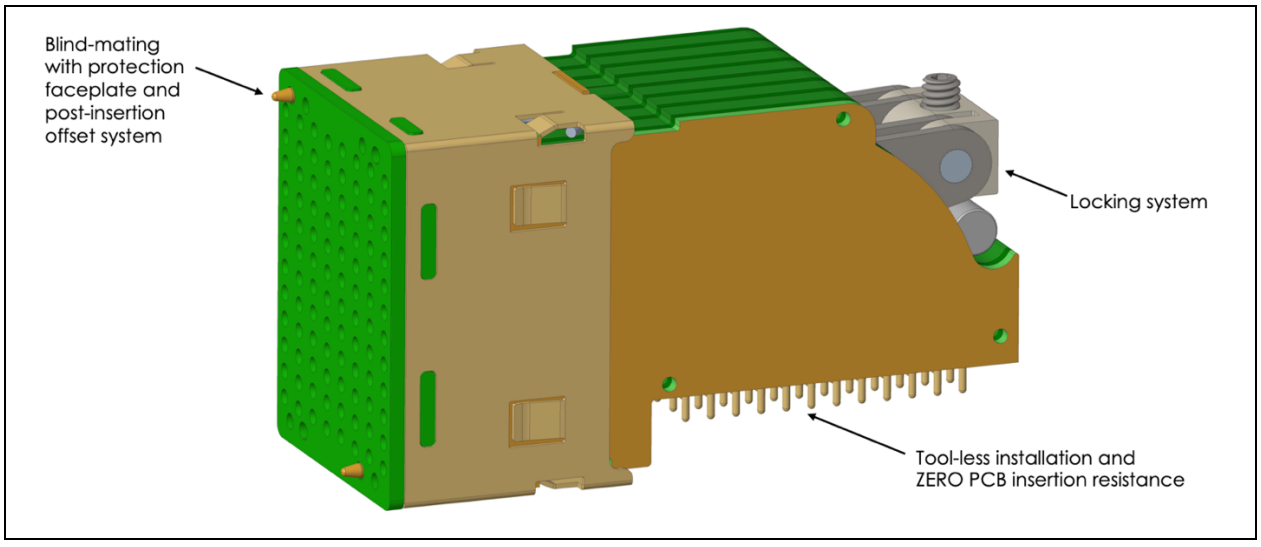

Fig. 4 HYPERBITS™ Single-Piece Connector which mounts on card without any insertion tools and blind-mates directly with the backplane

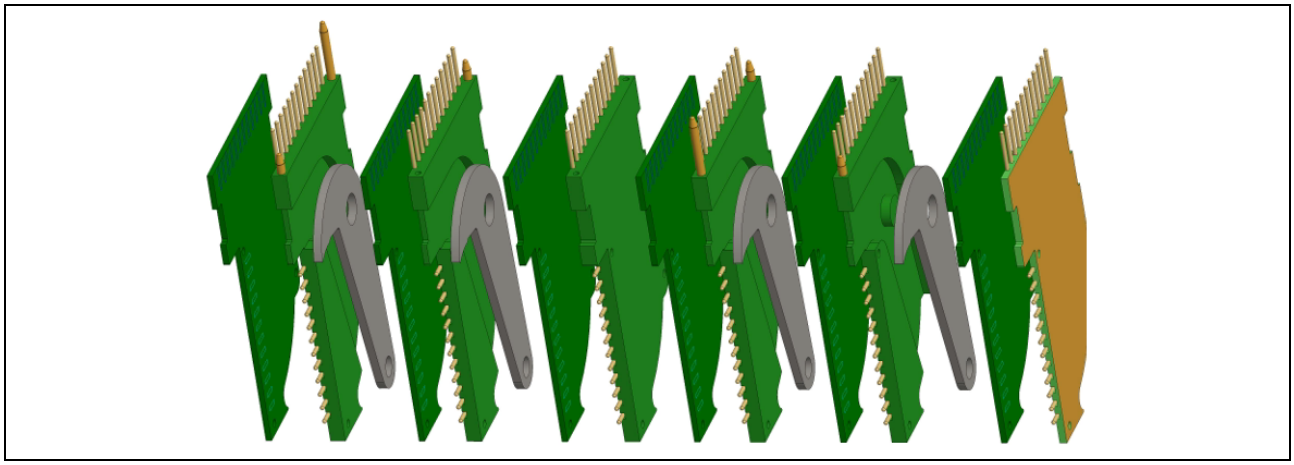

Fig. 5 Composite Internal Construction optimized for high data-rate transmission

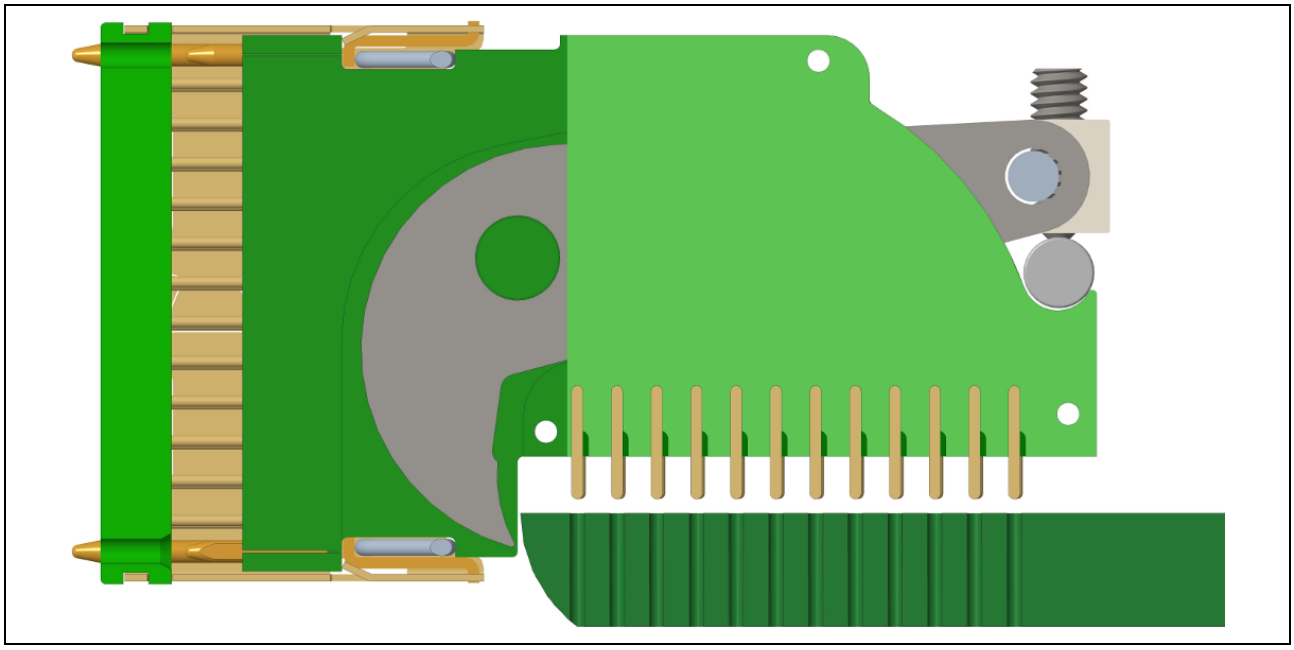

Fig. 6 Cross section into the connector showing the configuration of the internal locking and offsetting mechanism in UNLOCKED position

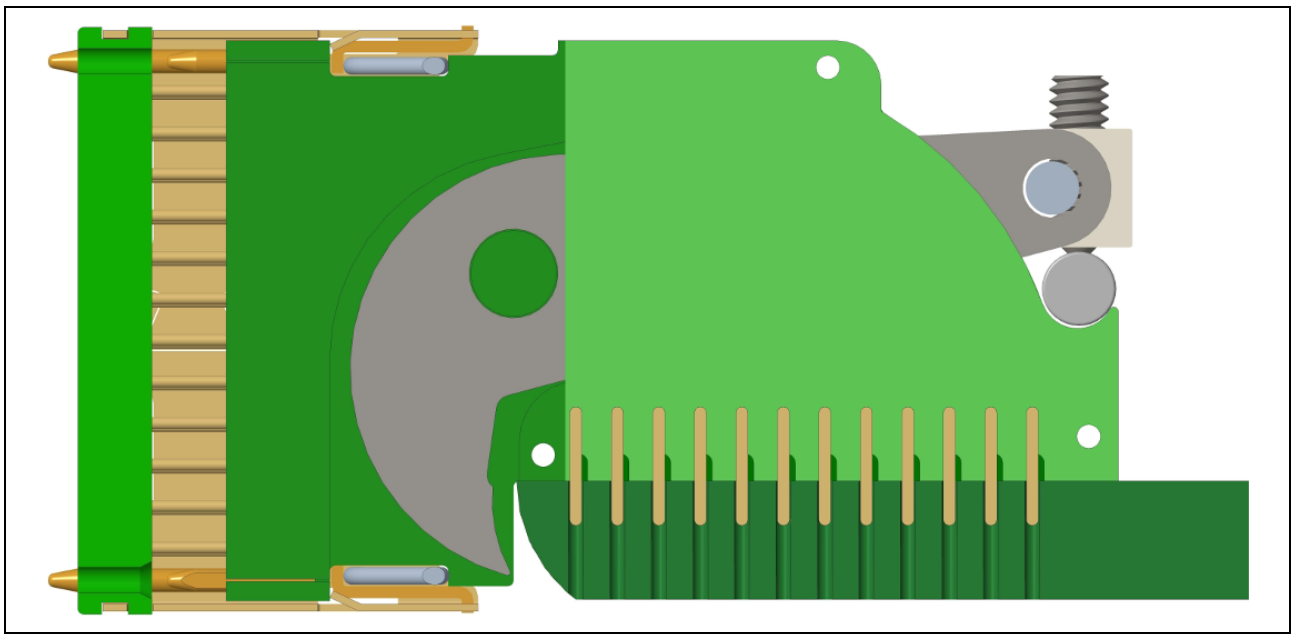

Fig. 7 Cross section showing the positioning of the connector into the PCB footprint with zero-force insertion

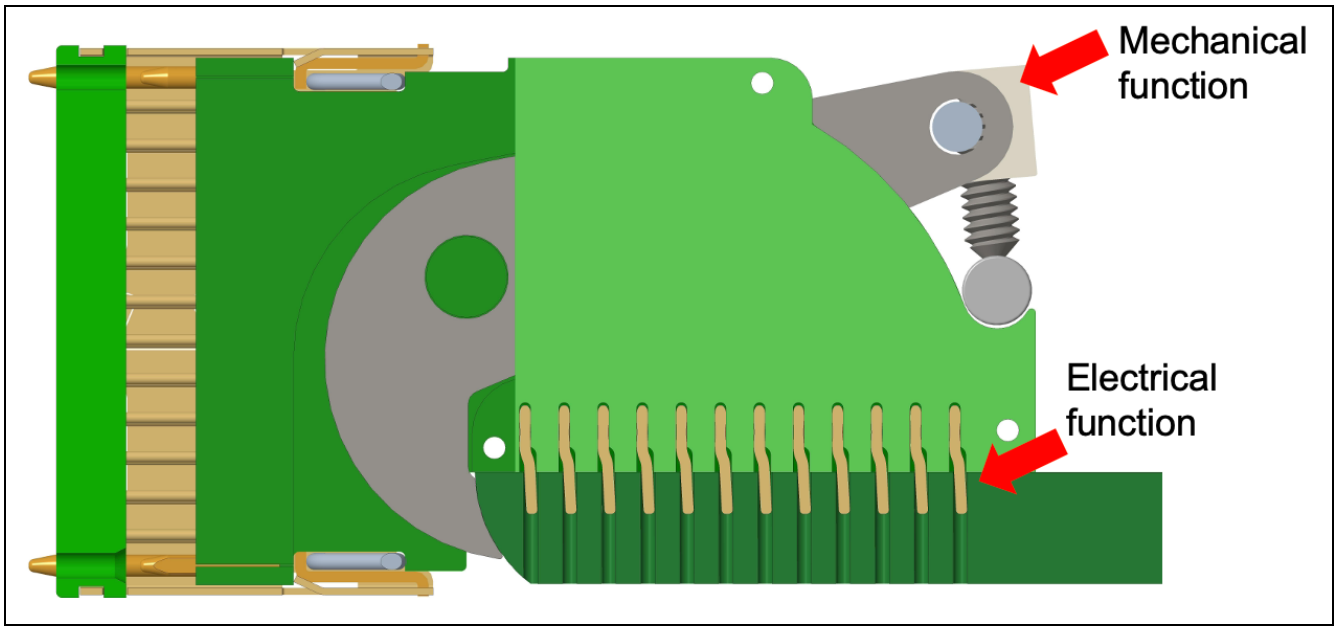

Fig. 8 – Cross-section showing the locking/offsetting lever in LOCKED position forcing the connector slightly forward activating the post-insertion offset principle in S-FECT™ Technology. The connector becomes mechanically attached to the PCB's front edge thereby separating the mechanical retention function from the contact terminations.

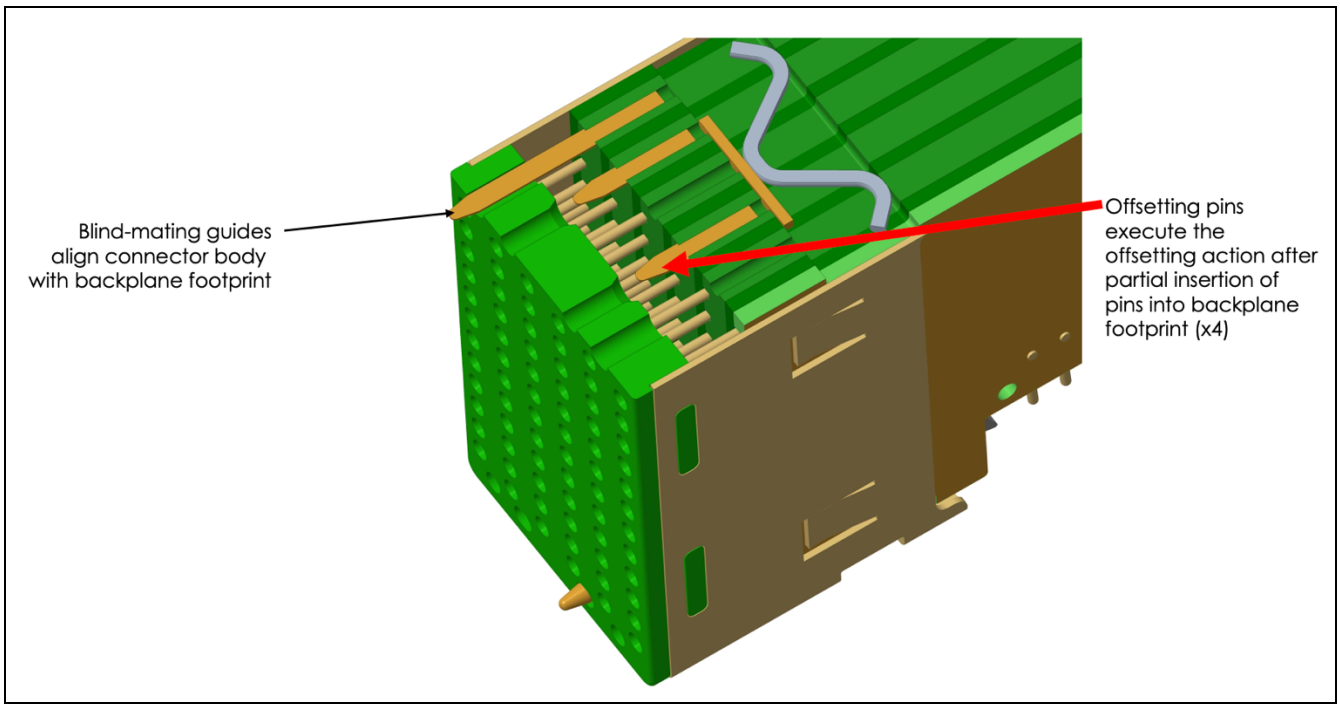

Fig. 9 - Cross-section into the connector face showing the protective post-insertion offsetting plate with blind-mating guides and offsetting pins

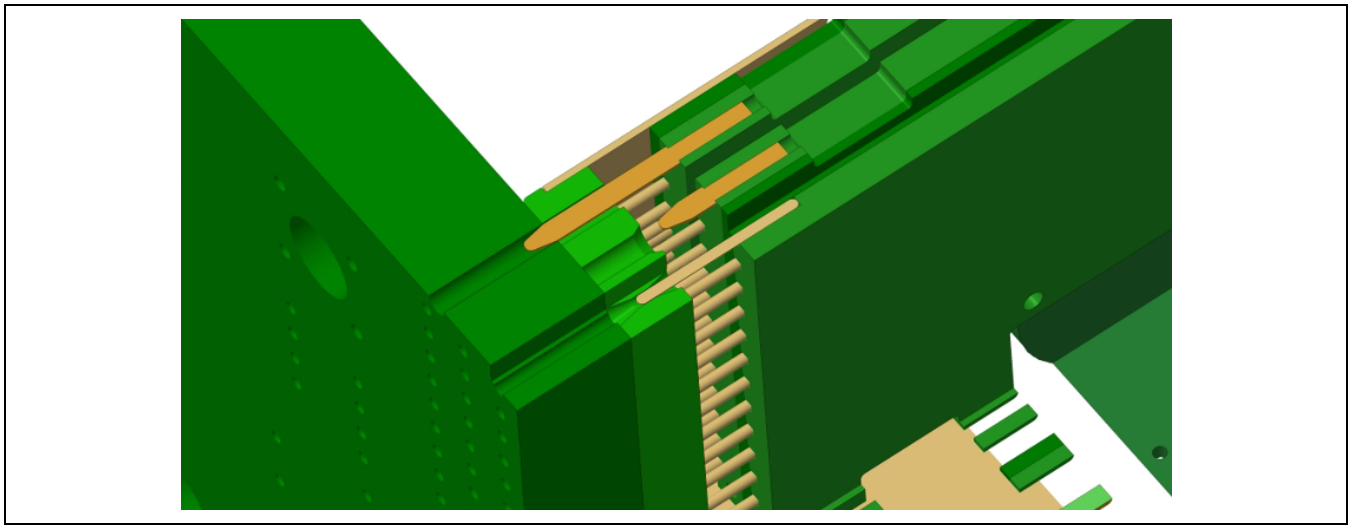

Fig. 10 – Blind mating – Step 1 Guides align connector body with footprint into backplane

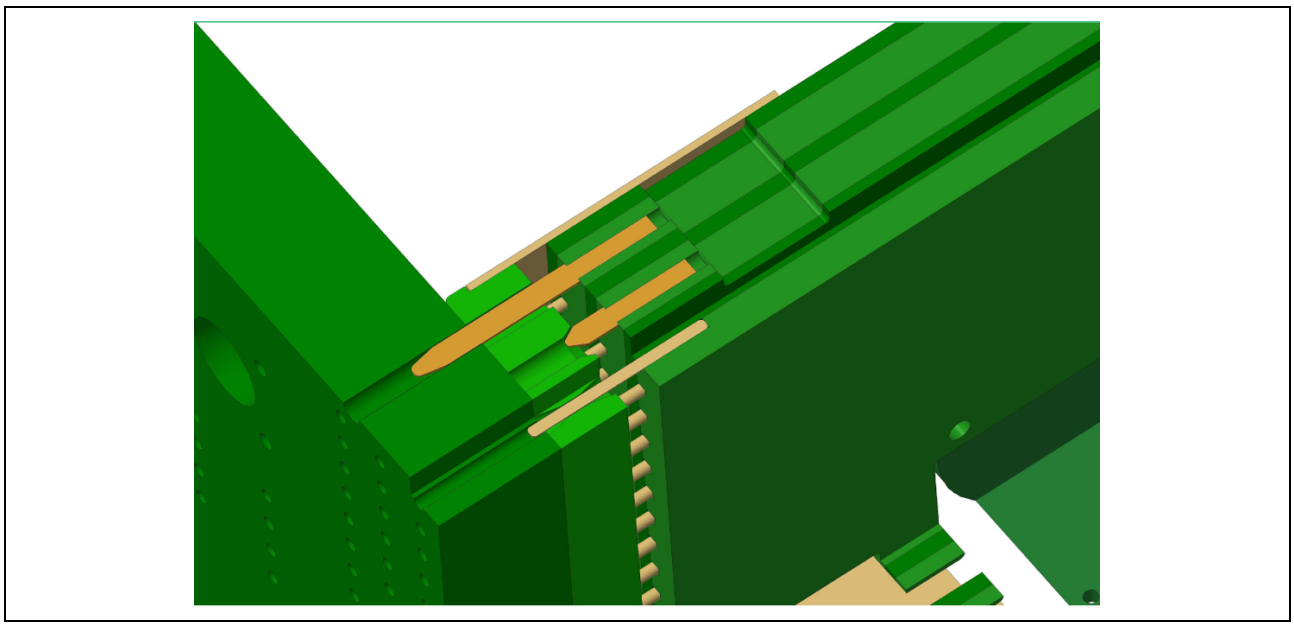

Fig. 11 – Blind mating – Step 2 contacts start entering into backplane

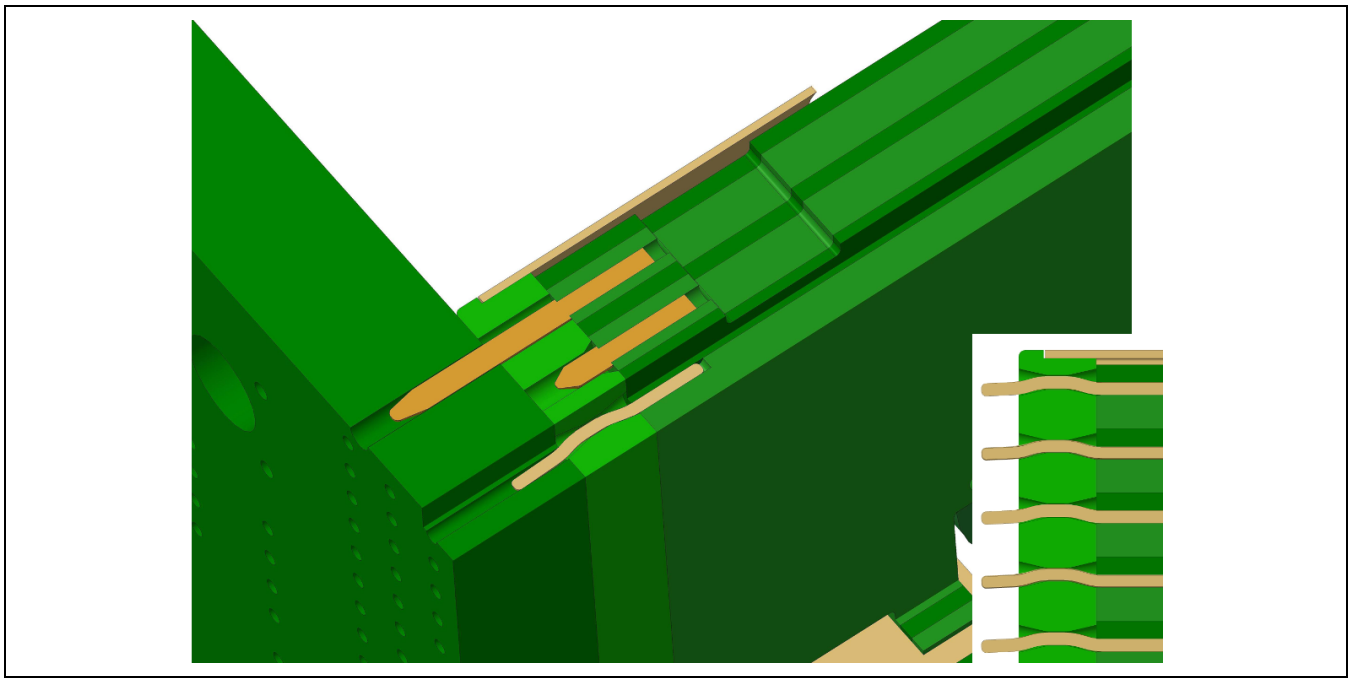

Fig. 12 – Blind mating – Step 3 offset fully achieved and locked over the offset pins

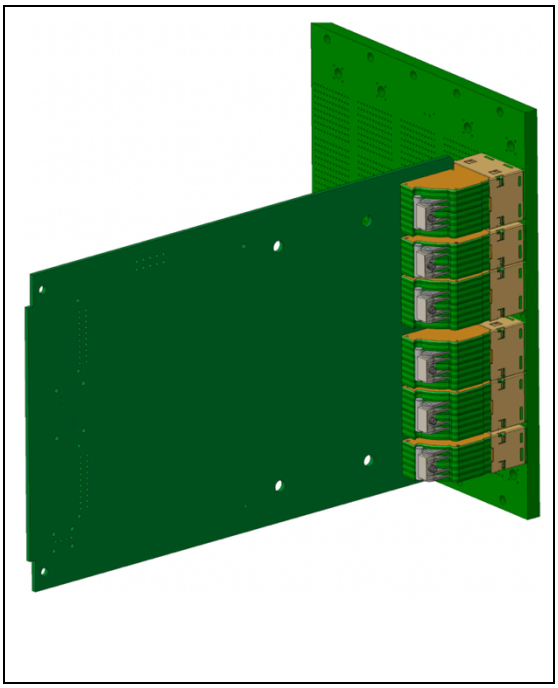

Fig. 13 – 3U system draft featuring two HYP1F600 and four HYP2F800 connectors per card

The design specifications

The latest HYPERBITS™ specifications compared to the requirements contained in the ADS specification document DOC-EEE-000218505 as shown in Table 1. This information may be updated for the final presentation in October 2022.

Table 1. Design Specifications of HYPERBITS™ compared to the ADS spec

Description	ADS spec	HYPERBITS™ spec	Condition / Comments
Plating thickness on contacts:	**1.27µm** minimum	**1.27µm** minimum	electroplated gold per ESCC23500 §3.3
Materials of concern:	Pure tin (Sn)	Pure Tin (Sn) NOT PRESENT	Not allowed
Mass:	to be supplied by MANUF	TBD	**Value remains TBD**
Operating temperature range:	-55°C to +125°C	**-65**°C to **+155**°C	Qualification temperature range is -55°C to +125°C
Marking	part number, date code	part number, date code	engraved or laser marked
Mating/Unmating cycles a)backplane b)card	500 cycles	1000 operations with a&b	Value tbd with MANUF per ESA/ESCC 3401 § 9.18
Mating/Unmating Force/contact a)backplane b)card	M 0.45N.st to 0.60N / U ≥0.15N	a) 0.6N max b) 0.01N	Per ESA/ESCC 3401 § 9.20 Mated and unmated 4 times **S-FECT ADVANTAGE**
Contact retention 5 pcs or 20% to be tested	4.4N for 6 sec.	4.4N for 6 sec.	ESA/ESCC 3401 § 9.17
Axial displacement MAX 0.3mm	10N for 6 sec.	10N for 6 sec.	ESA/ESCC 3401 § 9.17
High Speed Data Rate:	25 Gbps	25 Gbps	Differential signaling **Target is 35 Gbps**
Differential impedance:	**100Ω**	**Max 105Ω – Min 95Ω**	**+/- 5% target: 95Ω min and 105Ω max**
Contact resistance between mated contacts	20 mΩ	Not Applicable	ESA/ESCC 3401 § 9.1.1.3
Contact resistance between press-fit pin to PCB	300 µΩ MAX	Not Applicable	IPC 9797 §4.3.4 Test Method IEC 60512 test Method 2a. Measured during Qualification
Contact resistance between Slide-Fit Pin and PCB		≤ 5mΩ	**with a)backplane and with b)card**
Maximum resistance per line measured PCB to PCB	≤ 20.6mΩ	≤ 15mΩ	**From trace on backplane to trace on card including interfaces**
Current rating per contact:	**2A**	**2A**	1A minimum derated current over temperature range. **All contacts under load with maximum 30°C temperature rise.**
Working voltage	28V	96V at any altitude	
Insulation resistance	1 GΩ min	1 GΩ min	ESA/ESCC 3401 § 9.1.1.1 Test Method IEC 512-2, Test 3a, Method B. 500V +/- 50V
DWV	750 VRMS	750 VRMS	**Between PCBs**
Corona Effect	15VRMS	15VRMS	at 33000m per IEC-68-2-13
Back-drilling compatibility a)backplane b)card	required	a) YES b) YES	**MIN 1.6mm via depth from top of PCB**
S-Parameters – Insertion Loss – Cross talk – Capacitance – Inductance – Propagation Delay: **Targets provided in specification but actual values are TBD**			

Test Plan and Evaluation Activities

Alter Technology shall commence the evaluation activities of CPCI Serial commercial connectors and HYPERBITS™ connectors in December of 2022. The following information may be updated for the final presentation in October 2022.

The Test sequence is established to reach the confidence level required for the products. The tests shall be performed on the specified samples in the order shown in Figure 14.

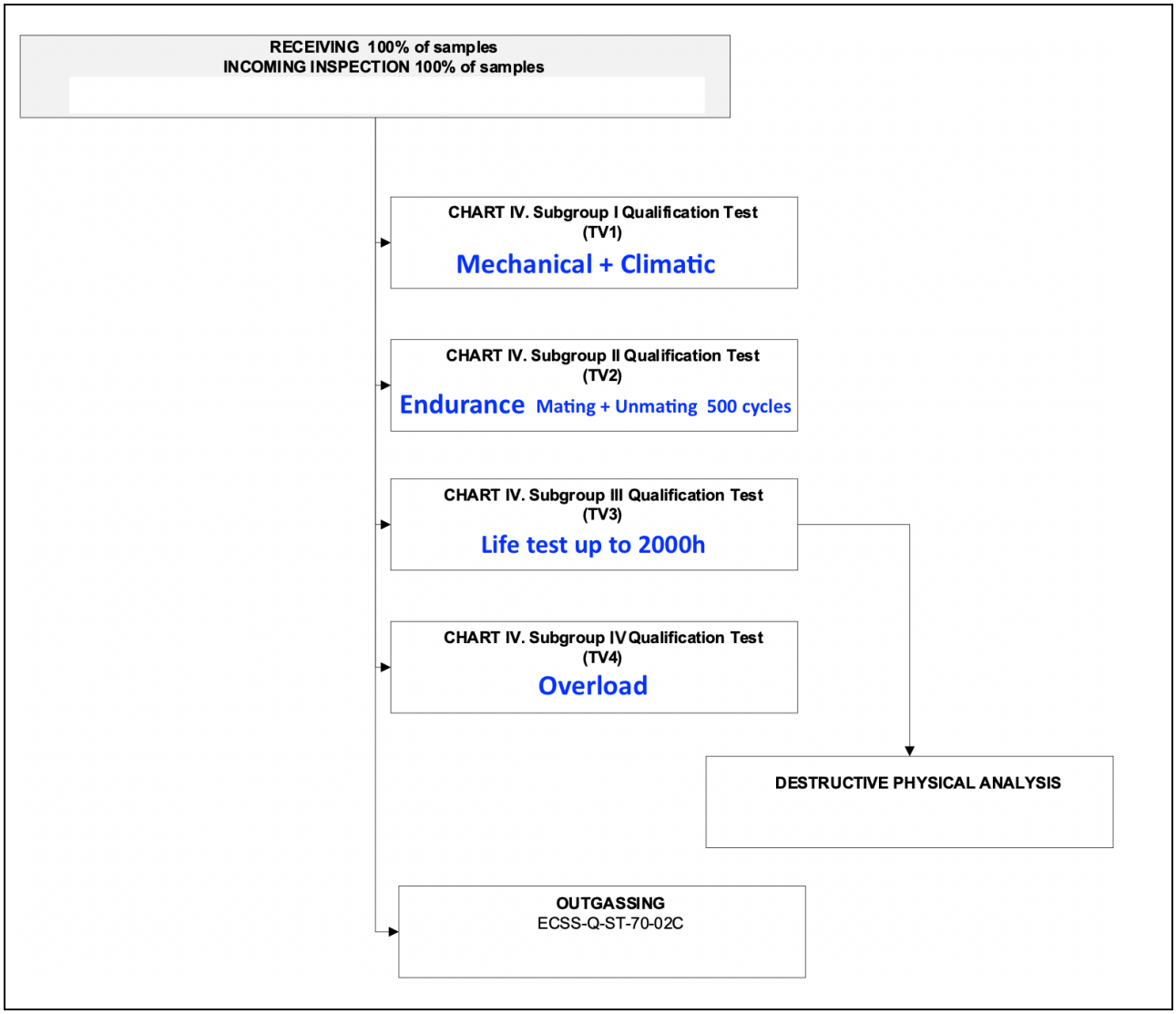

Fig. 14 – Test Sequence

Table 2 shows the test sequence to be performed, based on Chart IV - Qualification Test Subgroup I (TV1) of ESCC 3401 and additional requirements in DOC-EEE-000218505 Issue 2.

Table 2.

N.º	TEST	SAMPLES	TEST METHOD
1	External Visual Inspection	4 + control	ESCC 20500
2	PCB Insertion	4 + control	TBD (Note 1)
3	Electrical Measurement at Room Temperature	4 + control	TABLE II of Test Plan
4	External Visual Inspection	4 + control	ESCC 20500
5	Sine Vibration	4	ESCC 3401 Par. 9.11 (Notes 2 & 3)
6	External Visual Inspection	4 + control	ESCC 20500
7	Random Vibration	4	ESCC 3401 Par. 9.11 (Notes 2 & 4)
8	External Visual Inspection	4 + control	ESCC 20500
9	Mechanical Shock	4	ESCC 3401 Par. 9.12.1 (Notes 2 & 5)
10	External Visual Inspection	4 + control	ESCC 20500
11	Electrical Measurement at Room Temperature	4 + control	TABLE II of Test Plan
13	Thermal Shock	4	TABLE III of Test Plan
14	Electrical Measurement at Room Temperature	4 + control	TABLE II of Test Plan
15	External Visual Inspection	4 + control	ESCC 20500

Notes:

1. Instead of regular wiring test of the ESCC3401, Para. 9.10, press-fit mounting procedure shall be done: Press-fit connectors shall be inserted into the PCB. Details on mounting shall be provided by Manufacturer in each case. In the absence of those, insertion speed shall be between 25 mm/min and 50 mm/min as per NF EN60352-5, Para. 5.2.2.2.
   IPC Class 3 requirements shall be preferred for boards PCB manufacturing.
2. No impedance change or discontinuity of 1 ns or longer duration in accordance with EIA-364-87.
3. Sinusoidal Vibration
   Frequency range: 10-2000-10 Hz.
   Entire range from 10 Hz to 2000 Hz and return to 10 Hz in 30 mn.
   Amplitude: 1,5mm or 20g whichever is less.
   The cycle shall be performed in 3 mutual perpendicular direction total period of approximately 90 minutes.
4. Random Vibration
   Fda f1= 20 Hz
   f2 = 2000 Hz
   ASD of 0,2 g2/Hz
   Total test period 30 minutes
   The cycle shall be performed in 3 mutual perpendicular direction total period of approximately 90 minutes.
5. Mechanical Shock
   Shape of shock pulse: half-sine.
   A peak acceleration of 50 g with an 11 ms duration pulse.
   3 shocks in each direction along the 3 mutually perpendicular directions (i.e. 18 in total).

The Chart IV - Qualification Test Subgroup II (TV2) test sequence shall be performed on 4 samples in the order shown in Table 3, based on ESCC 3401 and additional requirements in DOC-EEE-000218505 Issue 2.

Table 3.

N.º	TEST	SAMPLES	TEST METHOD
1	External Visual Inspection	4 + control	ESCC 20500
2	PCB Insertion	4 + control	TBD (Note 1)
3	External Visual Inspection	4 + control	ESCC 20500
4	Electrical Measurement at Room Temperature	4 + control	TABLE II of Test Plan
5	Endurance until 50 times (Note 4)	4	ESCC 3401 Par. 9.18 (Notes 2 & 3)
6	Electrical Measurement at Room Temperature	4 + control	TABLE II of test Plan
7	Endurance until 500 times	4	ESCC 3401 Par. 9.18 (Notes 2 & 3)
8	Electrical Measurement at Room Temperature	4 + control	TABLE II of Test Plan
9	External Visual Inspection	4 + control	ESCC 20500

Notes:

1. Instead of regular wiring test of the ESCC3401, Para. 9.10, press-fit mounting procedure shall be done: Press-fit connectors shall be inserted into the PCB. Details on mounting shall be provided by Manufacturer in each case. In the absence of those, insertion speed shall be between 25 mm/min and 50 mm/min as per NF EN60352-5, Para. 5.2.2.2. IPC Class 3 requirements shall be preferred for boards PCB manufacturing.
2. This test is not applicable for the HyperBits (MindReach, FR) connectors due to the technology of the devices. Hence, it only applies for AirMaix connectors (Amphenol, USA).
3. Test conditions: 500 Cycles. A cycle is defined as one mating and one unmating. The coupling means shall be operated in a manner to simulate actual service. The plug and receptacle shall be completely separated during each cycle. The mating/unmating speed shall be 5 mm/second maximum and the cycling rate shall be 8 cycles/minute maximum.
4. Number of cycles for intermediate measurement of endurance test is TBC.

The Chart IV - Qualification Test Subgroup III (TV3) test sequence shall be performed on 4 samples in the order shown in Table 4, based on ESCC 3401 and additional requirements in DOC-EEE-000218505 Issue 2.

Table 4.

N.º	TEST	SAMPLES	TEST METHOD
1	External Visual Inspection	4 + control	ESCC 20500
2	PCB Insertion	4 + control	TBD (Note 1)
3	External Visual Inspection	4 + control	ESCC 20500
4	Electrical Measurements at room temperature	4 + control	TABLE VII of Test Plan
5	Electrical Measurements at high temperature	4	TABLE VIII of Test Plan
6	Electrical Measurements at low temperature	4	TABLE IX of Test Plan
7	Life test (until 500 h)	4	TABLE VII of Test Plan
8	Electrical Measurements at room temperature	4 + control	TABLE VII of Test Plan
9	Electrical Measurements at high temperature	4	TABLE VIII of Test Plan
10	Electrical Measurements at low temperature	4	TABLE IX of Test Plan
11	Life test (until 1000 h)	4	TABLE VII of Test Plan
12	Electrical Measurements at room temperature	4 + control	TABLE VII of Test Plan
13	Electrical Measurements at high temperature	4	TABLE VIII of Test Plan
14	Electrical Measurements at low temperature	4	TABLE IX of Test Plan
15	Life test (until 2000 h)	4	TABLE VII of Test Plan
16	Electrical Measurement at Room Temperature	4 + control	TABLE VII of Test Plan
17	Electrical Measurements at high temperature	4	TABLE VIII of Test Plan
18	Electrical Measurements at low temperature	4	TABLE IX of Test Plan
19	External Visual Inspection	4 + control	ESCC 20500

Note:

1. Instead of regular wiring test of the ESCC3401, Para. 9.10, press-fit mounting procedure shall be done: Press-fit connectors shall be inserted into the PCB. Details on mounting shall be provided by Manufacturer in each case. In the absence of those, insertion speed shall be between 25 mm/min and 50 mm/min as per NF EN60352-5, Para. 5.2.2.2. IPC Class 3 requirements shall be preferred for boards PCB manufacturing.

Destructive Physical Analysis shall be performed on 4 samples from Chart IV – Qualification Test Subgroup III in the order shown in Table 5, based on ESCC 21001.

Table 5.

N.º	TEST	SAMPLES	TEST METHOD
1	External Visual Inspection	4	ESCC 20500
2	Lead Material Verification (Note 1)	1	ESCC 20500
3	Radiographic Inspection	4	ESCC 20900
4	Marking Permanence	4	ESCC 24800
5	Cross Section (Note 2)	4	ESCC 20400

Notes:
1. One piece of each version.
2. The inspection shall:
   - Confirm that the contact retention clips are correctly installed.
   - Confirm that there are no broken or damaged contact retention clip tangs.
   - Any plating(s) are continuous and bonded to the underlying material.
   - Confirm that the connector shell is bonded to the connector insert.

The Chat IV - Qualification Test Subgroup IV (TV4) test sequence shall be performed on 4 samples in the order shown in Table 6, based on ESCC 3401 and additional requirements in DOC-EEE-000218505 Issue 2.

Table 6.

N.º	TEST	SAMPLES	TEST METHOD
1	External Visual Inspection	4 + control	ESCC 20500
2	PCB Insertion	4 + control	TBD (Note 1)
3	External Visual Inspection	4 + control	ESCC 20500
4	Electrical Measurement at Room Temperature	4 + control	TABLE II of Test Plan
5	High Temperature Measurements	4	TABLE XII of Test Plan
6	Electrical Measurement at Room Temperature	4 + control	TABLE II of Test Plan
7	External Visual Inspection	4 + control	ESCC 20500
8	Overload Test	4	TABLE XI of Test Plan
9	Electrical Measurement at Room Temperature	4 + control	TABLE II of Test Plan
10	External Visual Inspection	4 + control	ESCC 20500

Note:
1. Instead of regular wiring test of the ESCC3401, Para. 9.10, press-fit mounting procedure shall be done: Press-fit connectors shall be inserted into the PCB. Details on mounting shall be provided by Manufacturer in each case. In the absence of those, insertion speed shall be between 25 mm/min and 50 mm/min as per NF EN60352-5, Para. 5.2.2.2. IPC Class 3 requirements shall be preferred for boards PCB manufacturing.

Conclusion

Establishing a valid interface technology for the next generations of embedded electronics in space flight applications is a long and difficult process, however the efforts are well worth the investment from interested parties in the space community.
This exercise will represent a significant first step in the path towards the full qualification of interconnect devices for CPCI Serial Space systems.

Abbreviations and Acronyms

ADHA – Advanced Data Handling Architecture
ADS – Airbus Defense and Space
ARTES – Advanced Research in Telecommunication Systems
CPCI – Compact PCI – Compact Peripheral Component Interface
ESA – European Space Agency
ESCC – European Space Components Coordination
i2i – imagination 2 innovation (MINDREACH motto)
IPC – Institute for Printed Circuits
PCB – Printed Circuit Board
PCI - Peripheral Component Interface
PICMG – PCI Industrial Computers Manufacturers Group
PTH – printed through hole
S-FECT – Slide-Fit Electrical Contact Termination
VME – Versa Module Eurocard (computer bus standard)
VPX – VME plus PCI and "X" from extents, meaning a combination of both bus standards

REFERENCES

[1] CompactPCI® Connectors In Space Flight Applications, Prepared By: Richard Williams (Code 562) Kusum Sahu (Code 562), Reviewed By: Dr. Henning Leidecker, (Code 562) Terry King (Code 562) Dr. John Day (Code 560) AETD cPCI Review Committee, August 3, 2007, published
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AUTHORS

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President at PERFORMANCE INTERCONNECT SAS
Technology & Relationship Development Adviser at MINDREACH i2i SL

With over 20 years of experience in the connector industry Mr. Mindreci is an innovator in low-force solderless connection methods for power and high-speed contact technology in harsh environments. Mr. Mindreci is the principal inventor of the HYPERBITS™ connector and the principal inventor of S-FECT™ Technology, a non-destructive, solderless interface system used between signal contacts and PCBs.

Formerly the director of sales in EMEA and captain of the global innovation team at Positronic (prior to the acquisition by Amphenol in 2021), Mr. Mindreci has been a member of the PICMG CPCI Serial Space workgroup during 2017 and between 2016 and 2021 has contributed to developments supported by CNES and ESA towards completion of ESCC detail specifications 3401/98 and 3401/99 and qualification of low-force compliant press-fit termination technology for D-Subminiature connectors to ESCC 3401.

Mr. Dimas Morilla

Technical Support Manager Parts Laboratory Department
at ALTER TECHNOLOGY TÜV NORD S.A.U.

Employed at ALTER TECHNOLOGY since 2002, Mr. Morilla accumulated significant experience in environmental and reliability testing for EEE components and offered technical support to multiple ESA missions.

Formerly the Technical Manager of Receiving/Incoming Testing and DPA-FA sections, he currently holds the position of Technical Support Manager responsible for the growth and adaptation of Alter's parts laboratory capabilities to new requirements and to offer ongoing technical assistance to internal and external customers.

Dimas holds a master's degree in physics and is certified for Pre-Encapsulation Customer Source Inspection of EEE Components, performance of Constructional Analysis Tests, Screening, Counterfeit Detection, Destructive Physical Analysis and Failure Analysis.